In the Claims

Please amend the claims as follows:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Previously presented) The timing recovery loop as recited in claim 19, further comprising finite impulse response (FIR) filters electrically coupling the carrier recovery circuits to the forward equalizers.

5. (Previously presented) The timing recovery loop as recited in claim 4, wherein the FIR filters are square-root raised cosine filters.

6. (Previously presented) A digital receiver connected to N antennae including N timing recovery loops electrically coupled to the N antennae, each of the N timing recovery loops constructed as recited in claim 7.

7. (Currently amended) A timing recovery loop in the front end of a digital receiver including N antennae, comprising:

N sample rate converters, each receiving an Nth symbol stream at a first sampling rate from an Nth antenna and ~~outputs~~ outputting the Nth symbol stream at a second sampling rate responsive to a timing recover (TR) control signal;

N forward equalizers, each generating an Nth equalized feedback signal based on the Nth symbol stream at the second sampling rate, respectively; and

a timing recovery circuit generating the TR control signal based upon a combination of the N equalized feedback signals, wherein the combination is used to generate an output of the digital receiver .

8. (Original) The timing recovery loop as recited in claim 7, further comprising N carrier recovery circuits, each electrically coupling an Nth one of the N sample rate converters to an Nth one of the forward equalizers.

9. (Original) The timing recovery loop as recited in claim 8, further comprising N finite impulse response (FIR) filters, each electrically coupling an Nth one of the carrier recovery circuits to an Nth one of the forward equalizers.

10. (Original) The timing recovery loop as recited in claim 9, wherein each of the N FIR filters is a square-root raised cosine filter.

11. (Currently amended) A timing recovery loop in the front end of a digital receiver including N antennae, comprising:

N sample rate converters, each receiving an Nth symbol stream at a first sampling rate from an Nth antenna and outputting the Nth symbol stream at a second sampling rate responsive to a timing recovery (TR) control signal;

N forward equalizers, each generating an Nth equalized feedback signal based on the Nth symbol stream at the second sampling rate, respectively;

a timing recovery circuit generating the TR control signal based upon a selected one of the N equalized feedback signals, wherein the selection is controlled based on a combination of the N equalized feedback signals, the combination used to generate an output of the digital receiver; and

N carrier recovery circuits, each electrically coupling an Nth one of the N sample rate converters to an Nth one of the forward equalizers.

12. (Canceled)

13. (Previously presented) The timing recovery loop as recited in claim 11, further comprising N finite impulse response (FIR) filters, each electrically coupling an Nth one of the carrier recovery circuits to an Nth one of the forward equalizers.

14. (Original) The timing recovery loop as recited in claim 13, wherein each of the N FIR filters is a square-root raised cosine filter.

15. (Original) The timing recovery loop as recited in claim 11, further comprising a selector receiving N signals based on the N equalized feedback signals at N respective input terminals and applying the selected one of the N signals to the timing recovery circuit.

16. (Canceled)

17. (Currently amended) A method for operating a digital receiver, including N sample rate converters responsive to a timing recovery (TR) control signal, connected to N antennae, respectively, comprising:

generating N equalized feedback signals, each based on an Nth symbol stream having a controlled sample rate;

combining the N equalized feedback ~~signal~~ signals to produce a combined equalized feedback signal, wherein the combined equalized feedback signal is used to generate an output of the digital receiver;

producing the TR control signal based on the combined equalized feedback signal; and

applying the TR control signal to the sample rate converters to thereby permit the N sample rate converters to output N symbol streams at the controlled sample rate.

18. (Canceled)

19. (Previously presented) The timing recovery loop as recited in claim 7, further comprising carrier recovery circuits electrically coupling the sample rate converters to the forward equalizers.